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| | | | | | | (Date) | |
| APPLICATION NO. | FILING DATE | | FIRST NAME | D INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. | |
| 10/605,258 | 09/18/2003 | | JOHN B | RULEY | FIS920030145US1 | 2257 | |
| ritle of invention: Si | ITE-SPECIFIC METHODO | LOGY FOR LOCA | ALIZATION | AND ANALYZING JUNCTION | ON DEFECTS IN MOSFET | DEVICES | |
| APPLN. TYPE | SMALL ENTITY | ISSUE FEE | | PUBLICATION FEE | TOTAL FEE(S) DUE | DATE DUE | |
| nonprovisional | NO | \$1370 | | \$300 | \$1670 | 02/15/2005 | |
| EXAMINER ART UT | | | IT | CLASS-SUBCLASS |] | | |
| DANG, | 2818 | | 438-014000 | | | | |
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| Authorized Signature | Walt | 2 | | Date | November 8, 20 | | |
| Typed or printed name Peter W. Peterson | | | | Registration | No. 31,867 | | |

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